

# Cole Drake

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## EDUCATION

**Carnegie Mellon University**

**Bachelor of Science in Electrical and Computer Engineering, Minor in Robotics**

**Pittsburgh, PA**

**Expected May 2027**

**Relevant Coursework:** Computer Systems, Computer Architecture, Structure and Design of Digital Systems, Logic Design and Verification

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## WORK EXPERIENCE

**WiseLab**

**September 2025 – Present**

**Hardware Research Intern**

**Pittsburgh, PA**

- Building a synchronized 4-camera capture system (1080p @ 60 FPS) with OpenCV intrinsic/extrinsic calibration for multi-view alignment
- Developed the capture, synchronization, and preprocessing pipeline feeding 3D scene reconstruction
- Trained and tuned a PyTorch neural point-based graphics model (NPBG), adding a point-sampling stage to reduce rendering compute
- Optimized the model and rendering by adding in a sampling model to reduce compute

**Meta Mobility Lab**

**April 2025 – April 2026**

**Machine Learning Researcher**

**Pittsburgh, PA**

- Led 150+ hours of real-world validation of a hip exoskeleton control system integrating IMUs, motor encoders, and foot pressure sensors
- Analyzed multi-sensor data in Python to identify failure modes across 3 control model iterations deployed on NVIDIA Jetson
- Expanded operating range from 1.0 m/s on flat ground to 0.4–1.4 m/s across  $\pm 12^\circ$  inclines, reducing control error by ~90%

**Carnegie Mellon Racing Team**

**August 2023 - August 2025**

**Gear Systems Lead**

**Pittsburgh, PA**

- Delivered a 1:13 planetary gear system meeting torque and packaging constraints, cutting weight 8% through iterative redesign
  - Coordinated with manufacturing and mechanical teams to resolve integration issues through final assembly
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## PROJECTS

**RISC-V Processor Microarchitecture**

**May 2026 - Present**

**Verification and Design Project**

- Extended the open-source Ibex RISC-V core with branch prediction, L1 I/D caches, and 14 new performance counter events, achieving a  $3.06\times$  speedup (IPC 0.150  $\rightarrow$  0.457) across 11 workloads
- Designed ~2,300 lines of SystemVerilog RTL: 6 branch predictors (up to 94% accuracy) with a RAS and BTB, and parameterized set-associative caches with configurable replacement, write policy, and next-line prefetch
- Adapted the CV32E40P verification environment for Ibex with 4 checkers, 32 SVA assertions, and 100 coverage bins; automated a 776-simulation regression across 10 configurations with 100% coverage closure
- Ran 11 design-space studies (CPI, MPKI, miss rates) showing caches drove  $2.9\times$  vs. 5.5% from prediction; diagnosed a cache-conflict pathology fixed by 4-way associativity ( $2.6\times$  on the affected workload)

**Pipelined Matrix-Vector Multiplier**

**November 2025**

**SystemVerilog, Vivado, Spartan-7 FPGA**

- Designed a pipelined multiply-accumulate engine computing a  $128\times 128$  matrix-vector product in 521 cycles, within 2% of the 512-cycle theoretical minimum
  - Replicated operand ROMs across 36 dual-port BRAMs to feed 32 DSP multipliers in parallel (32 MACs/clock, ~99% of on-chip BRAM)
  - Met 100 MHz timing (+1.01 ns WNS) by registering each level of a 5-stage adder tree; overlapped the bias-vector reduction to add zero cycles
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## SKILLS

**Languages:** SystemVerilog, Verilog, C, C++, Python, Java, Javascript, SQL

**Hardware/Systems:** RTL Design, Digital Design, FPGA, UVM, Testbench Development, SVA, Embedded systems

**Tools:** Vivado, Quartus, Linux, Git, OpenCV, PyTorch, NVIDIA Jetson, MATLAB, ANSYS